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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,193	01/08/2001	Chun-Gi You	06192.0155.NPUS00	4881

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EXAMINER
BREWSTER, WILLIAM M

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 09/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/755,193	YOU, CHUN-GI	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40 and 42-46* is/are pending in the application.

4a) Of the above claim(s) *1-9 and 14-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-13,40 and 42-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10-13, 40, 42-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al., U.S. Patent No. 2002/0061410 A1, in view of Park et al., U.S. Patent No. 5,478,766.

Sasaki teaches a contact structure of a wire, comprising: in fig. 1, a gate wire 5 made of a first conductive material on an insulating substrate 2; where the wire has a flat surface, a gate insulating layer 4 covering the gate wire; a semiconductor layer 5 formed on the gate insulating layer; a data wire 14 including a second conductive material on the gate insulating layer and the semiconductor layer; a passivation layer 9 covering the data wire; and a transparent conductive layer 13 pattern directly contacting with and connected to the gate wire or the data wire 14 through a first contact hole 12 of the gate insulating layer or the passivation layer; wherein and the passivation layer are made of silicon-nitride, p. 2, ¶ 33; wherein the transparent conductive layer pattern is made of indium zinc oxide, p. 2, ¶ 29 and 33; wherein the passivation layer further comprises a second contact hole exposing the data pad 10 and a third contact hole 15

exposing the gate pad along with the gate insulating layer, the first to the third contact holes have a shape including rounds or corner.

Although Sasaki does not specify the material for the insulation film, it is reasonable that a silicon nitride as specified for the passivation film would be used, as this would simplify processing.

Sasaki does not teach a data wire including a second conductive layer includes aluminum-based conductive materials, but Park does. Park teaches the thin film transistor comprising forming in fig. 3A, a gate wire 2, 10 including a first conductive layer on an insulating substrate 1; a gate insulating layer 3 covering the gate wire; a semiconductor layer 5 formed on the gate insulating layer; a data wire 7, 11 including a second conductive layer on the gate insulating layer and the semiconductor layer; a passivation layer 14 covering the data wire, col. 2, line 12 - col. 3, line 18; wherein the first conductive layer or the second conductive layer includes metal containing an aluminum-based material, also see fig. 4, col. 3, lines 19-33. Though Park does not bother forming interconnect lines through contact holes, this is inherent, as the source, drain, and gate electrodes must be connected for signals to be processed. Park gives motivation in col. 3, lines 41-48. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Park's process with Sasaki's invention would have been beneficial because the semiconductor is isolated from a data line to inhibit an optical current leakage

Sasaki and Park do not specify the size of the contact holes to be greater than 4 μm x 4 μm, but these dimensions may be optimized by the user.

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentablility to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art . . . such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality . . . More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

In re Aller 105 USPQ 233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Claims 45 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki in view of Park as applied to claims 40, 42-44 above, and further in view of Yamada, et al., U.S. Patent No. 6,072,450.

Sasaki does not specify the wiring layout of the TFT array panel, but Yamada does.

Yamada teaches the thin film transistor array panel, in fig. 1, wherein the gate wire includes a gate line, a gate electrode 4A connected to the gate line 4, and a gate pad (not labeled, but part of 4) which is connected to the gate line and receives a signal from an external circuit, and the data wire includes a data line 13, a source electrode 7B connected to the data line, a drain electrode 7B separated from the drain electrode and opposite to the drain electrode with the respect to the gate electrode, and a data pad 14A that is connected to the data line and receives a signal from a external circuit, col. 5, line 37 - col. 6, line 44. Yamada gives motivation in col. 2, line 66 - col. 3, line 3. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Yamada's process with Sasaki's invention would have been beneficial because it helps achieve a high luminescence at a low voltage.

Response to Arguments

Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

In view of the amendments of the applicant, Sasaki teaches the formation of the gate wire, semiconductor layer, passivation layer, and transparent conductive layer pattern directly connected to the data wire. Sasaki does not teach using a second conductive layer with an aluminum-based material, but Park does in figs. 3 and 4.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 703-305-5906. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-3432 for regular communications and 703-305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

WB
August 19, 2003

W. David Coleman
Primary Examiner